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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/812,668	03/20/2001	Yasuhiro Koizumi	19036/37209	2502

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EXAMINER
HASSANZADEH, PARVIZ

ART UNIT	PAPER NUMBER
1763	

DATE MAILED: 09/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/812,668	KOIZUMI ET AL.	
	Examiner	Art Unit	
	Parviz Hassanzadeh	1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *6,7,9-11,13-16 and 18-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8,12,17,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

The drawings were received on 8/7/03. These drawings are acceptable by the Examiner.

Claim Missing

Page 11 of the amendment receive on 8/27/03 is missing.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-5, 8, 12, 17, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (Fig. 4, pages 1-3) in view of Gorin (US Patent No. 4,464,223).

The admitted prior art (Fig. 4) teaches a conventional ion plating apparatus 60 comprising:

a vacuum chamber 61;

a substrate holder 62 for holding a substrate 65; and

a power supply unit including an RF power supply 66 coupled to the target 62 for generating a plasma, and a DC bias power supply 67 for applying a negative bias voltage on the substrate holder 62.

The admitted prior art fails to teach the bias power supply having a pulse bias component corresponding to a pulse output having a positive value for a predetermined time, with a cycle set in a range of 1KHz to 1GHz.

Gorin teaches a plasma processing apparatus (Fig. 2) including a bias supply unit comprising a DC power supply 42 and an RF power source 36 wherein the DC and the AC voltage are simultaneously applied to a substrate holder 14, wherein the RF AC power supply 36 outputs a frequency of 100 kHz. The amount of the RF power source 36 directly affect the etch rate (rate of ions reaching the substrate) and the DC power source allows the amount of DC biasing by plasma to be changed independently of the pressure or power (column 2, line 6 through column 3, line 16).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the bias mechanism as taught by Gorin in the apparatus of the admitted prior art in order to enhance attraction of plasma species toward the substrate.

Further regarding claim 2, 3, 17 (the ratio of the predetermined time of the pulse bias to the cycle of the bias voltage): the AC/DC power of the biasing mechanism of Gorin is capable of being adjusted to a desire value.

Further regarding claims 3, 4 (the pulse bias being a square wave pulse): the AC and square wave generators are considered as art recognized equivalent for the same purpose of generating a time-varying (pulsing) voltage. See MPEP 2144.06, Art Recognized Equivalent for the Same Purpose, Substituting Equivalents Known for the Same Purpose (*in re Fout*, 675 F.2d 297, 213 USPQ 532 (CCPA 1982)).

Further regarding claims 8, 12 (low pass filter and band pass filter): the use of filters between the plasma power source and the bias power source is considered a well known feature in the art and the employment of such filters would have been obvious to one of ordinary skill in the art for the purpose of eliminating the output from one source reaching and interfering with the other source.

Claims 1-5, 8, 12, 17, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (Fig. 4, pages 1-3) in view of Okano et al (JP 56-81678 A) and Gorin (US Patent No. 4,464,223).

The admitted prior art (Fig. 4) teaches a conventional ion plating apparatus 60 comprising:

a vacuum chamber 61;

a substrate holder 62 for holding a substrate 65; and

a power supply unit including an RF power supply 66 coupled to the target 62 for generating a plasma, and a DC bias power supply 67 for applying a negative bias voltage on the substrate holder 62.

The admitted prior art fails to teach the bias power supply having a pulse bias component corresponding to a pulse output having a positive value for a predetermined time, with a cycle set in a range of 1KHz to 1GHz.

Okano et al teach a plasma processing apparatus (Fig. 5) including a bias supply unit comprising a DC power source 35 and an RF power source 33 wherein the DC voltage is adjusted by the superimposed AC voltage on the substrate holder 25 (Abstract).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the adjustable bias mechanism as taught by Okano et al in the apparatus of the admitted prior art in order to adjust and thus control the bias voltage applied to the substrate holder.

The admitted prior art in view of Okano et al fail to teach the bias power supply having a pulse bias component corresponding to a pulse output having a positive value for a predetermined time, with a cycle set in a range of 1KHz to 1GHz.

Gorin teaches a plasma processing apparatus (Fig. 2) including a bias supply unit comprising a DC power supply 42 and an RF power source 36 wherein the DC and the AC voltage are simultaneously applied to a substrate holder 14, wherein the RF AC power supply 36 outputs a frequency of 100 kHz. The amount of the RF power source 36 directly affect the etch rate (rate of ions reaching the substrate) and the DC power source allows the amount of DC

biasing by plasma to be changed independently of the pressure or power (column 2, line 6 through column 3, line 16).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use the AC power source 36 as taught by Gorin in the apparatus of the admitted prior art in view of Okano et al as an art recognized equivalent for the same purpose of providing an RF AC source to a bias wafer support.

Further regarding claim 2, 3, 17 (the ratio of the predetermined time of the pulse bias to the cycle of the bias voltage): the ratio of the predetermined time can be controlled by changing the frequency of the AC power source.

Further regarding claims 3, 4 (the pulse bias being a square wave pulse): the AC and square wave generators are considered as art recognized equivalent for the same purpose of generating a time-varying (pulsing) voltage. See MPEP 2144.06, Art Recognized Equivalent for the Same Purpose, Substituting Equivalents Known for the Same Purpose (*in re Fout*, 675 F.2d 297, 213 USPQ 532 (CCPA 1982)).

Further regarding claims 8, 12 (low pass filter and band pass filter): the use of filters between the plasma power source and the bias power source is considered a well known feature in the art and the employment of such filters would have been obvious to one of ordinary skill in the art for the purpose of eliminating the output from one source reaching and interfering with the other source.

Claims 1-5, 8, 12, 17, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (Fig. 4, pages 1-3) in view of White (US Patent No. 4,039,416).

The admitted prior art (Fig. 4) teaches a conventional ion plating apparatus 60 comprising:

a vacuum chamber 61;

a substrate holder 62 for holding a substrate 65; and

a power supply unit including an RF power supply 66 coupled to the target 62 for generating a plasma, and a DC bias power supply 67 for applying a negative bias voltage on the substrate holder 62.

The admitted prior art fails to teach the bias power supply having a pulse bias component corresponding to a pulse output having a positive value for a predetermined time, with a cycle set in a range of 1KHz to 1GHz.

White teaches a plasma processing apparatus (Fig. 2) including a bias supply unit comprising a DC power source 33 and an RF power source 30 wherein the DC voltage is adjusted by the superimposed AC voltage on the substrate 31, wherein the DC supply provides a negative bias to the substrate and the RF supply can be operated at a frequency of 13.5 MHz and may be adjusted for a different application (column 2, lines 50-67).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the adjustable bias mechanism as taught by White in the apparatus of the admitted prior art in order to adjust and thus control the bias voltage applied to the substrate holder.

Further regarding claim 2, 3, 17 (the ratio of the predetermined time of the pulse bias to the cycle of the bias voltage): the ratio of the predetermined time can be controlled by changing the frequency of the AC power source.

Further regarding claims 3, 4 (the pulse bias being a square wave pulse): the AC and square wave generators are considered as art recognized equivalent for the same purpose of generating a time-varying (pulsing) voltage. See MPEP 2144.06, Art Recognized Equivalent for the Same Purpose, Substituting Equivalents Known for the Same Purpose (*in re Fout*, 675 F.2d 297, 213 USPQ 532 (CCPA 1982)).

Further regarding claims 8, 12 (low pass filter and band pass filter): the use of filters between the plasma power source and the bias power source is considered a well known feature in the art and the employment of such filters would have been obvious to one of ordinary skill in the art for the purpose of eliminating the output from one source reaching and interfering with the other source.

Claims 1-5, 8, 12, 17, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (Fig. 4, pages 1-3) in view of Yao et al (US Patent No. 6,051,114).

The admitted prior art (Fig. 4) teaches a conventional ion plating apparatus 60 comprising:

a vacuum chamber 61;

a substrate holder 62 for holding a substrate 65; and

a power supply unit including an RF power supply 66 coupled to the target 62 for generating a plasma, and a DC bias power supply 67 for applying a negative bias voltage on the substrate holder 62.

The admitted prior art fails to teach the bias power supply having a pulse bias component corresponding to a pulse output having a positive value for a predetermined time, with a cycle set in a range of 1KHz to 1GHz.

Yao et al teach a plasma processing apparatus (Fig. 1) including a pulsed DC power supply 48 providing a pulsed negative potential to a substrate holder 20 for alternatively accelerating the deposition flux toward the substrate or discharges the positive charges built up on the substrate. The pulsed DC bias method uses a pulsed voltage waveform to provide a nearly constant voltage to a substrate surface which provides uniform ion acceleration. The ion energy at the substrate surface is interrupted briefly when the pulsed DC waveform cycles to a slightly positive voltage as shown in Fig. 2 to remove charges building at the substrate surface. (column 4, lines 7-45) the frequency of the bias source may be selected at 30.5 MHz (column 9, lines 40-62).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the pulsed DC bias mechanism as taught by Yao et al in the apparatus of the admitted prior art in order to alternatively accelerate deposition ions toward the substrate or discharge positive charges built up on the substrate.

Further regarding claim 2, 3, 17 (the ratio of the predetermined time of the pulse bias to the cycle of the bias voltage): the ratio of the predetermined time can be controlled by changing the frequency of the AC power source.

Further regarding claims 3, 4 (the pulse bias being a square wave pulse): the AC and square wave generators are considered as art recognized equivalent for the same purpose of generating a time-varying (pulsing) voltage. See MPEP 2144.06, Art Recognized Equivalent for

the Same Purpose, Substituting Equivalents Known for the Same Purpose (*in re Fout*, 675 F.2d 297, 213 USPQ 532 (CCPA 1982)).

Further regarding claims 8, 12 (low pass filter and band pass filter): the use of filters between the plasma power source and the bias power source is considered a well known feature in the art and the employment of such filters would have been obvious to one of ordinary skill in the art for the purpose of eliminating the output from one source reaching and interfering with the other source.

Claims 1-5, 8, 12, 17, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (Fig. 4, pages 1-3) in view of Kofuji et al (US Patent No. 6,231,777 B1).

The admitted prior art (Fig. 4) teaches a conventional ion plating apparatus 60 comprising:

a vacuum chamber 61;

a substrate holder 62 for holding a substrate 65; and

a power supply unit including an RF power supply 66 coupled to the target 62 for generating a plasma, and a DC bias power supply 67 for applying a negative bias voltage on the substrate holder 62.

The admitted prior art fails to teach the bias power supply having a pulse bias component corresponding to a pulse output having a positive value for a predetermined time, with a cycle set in a range of 1KHz to 1GHz.

Kofuji et al teach a plasma processing apparatus (Fig. 33) wherein a pulsed bias potential is applied to a substrate support in order to suppress charge build-up on the substrate, wherein

the pulse voltage duty ratio may be selected to be 5% or below and repetition frequency being 400 KHz or above (abstract). The embodiment shown in Fig. 22 includes a pulsed voltage source 17 and a constant negative voltage source 25 and an amplifier 26 providing a pulsed biased potential as shown in Fig. 24 consisting of positive and negative potential cycles (column 7, line 14 through column 8, line 26).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the pulsed DC bias mechanism as taught by Kofuji et al in the apparatus of the admitted prior art in order to accelerate ions toward the substrate as well as to suppress positive charges built up on the substrate.

Further regarding claim 2, 3, 17 (the ratio of the predetermined time of the pulse bias to the cycle of the bias voltage): the ratio of the predetermined time can be controlled by changing the frequency of the AC power source.

Further regarding claims 3, 4 (the pulse bias being a square wave pulse): the AC and square wave generators are considered as art recognized equivalent for the same purpose of generating a time-varying (pulsing) voltage. See MPEP 2144.06, Art Recognized Equivalent for the Same Purpose, Substituting Equivalents Known for the Same Purpose (*in re Fout*, 675 F.2d 297, 213 USPQ 532 (CCPA 1982)).

Further regarding claims 8, 12 (low pass filter and band pass filter): the use of filters between the plasma power source and the bias power source is considered a well known feature in the art and the employment of such filters would have been obvious to one of ordinary skill in the art for the purpose of eliminating the output from one source reaching and interfering with the other source.

Response to Arguments

Applicant's arguments with respect to claims 1-5, 8, 12, 17, 21 and 22 have been considered but are moot in view of the new ground(s) of rejection.

The Applicants assert neither Okano et al nor Gorin teach the bias potential having positive and negative values as recited in claims 1 and 22.

The Examiner argues that the last limitation recited in the claims 1 and 22 are operational (step) limitations rather than structural limitation of the claimed apparatus and the apparatus of the prior art can be used to perform the recited steps. Furthermore, the recited limitation does not necessarily require the overall output of the bias power source having a positive and a negative potential, that is, the positive portion may just be high enough to be cancelled by the constant negative potential of the DC power source.

The Examiner has also introduced newly found prior arts teaching pulsed bias voltage source for applying positive and/or negative pulsed potential on a substrate support member.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sakamoto et al (JP 58-1000672) teach a plasma processing apparatus including an AC/DC superimposed power source for applying a pulsed bias voltage on a substrate holder 7 by an RF power source 11 and a DC power source 13 (Fig. 2);

Goring et al (US Patent No. 4,464,223) teach a plasma reactor including a bias power unit including an RF power source 36 and a DC power source 42 (Fig. 2);

Martin et al (US Patent No. 6,033,587) teach a plasma reactor including a bias system including an AC voltage superimposed on a DC current (Fig. 1);

Tomoyasu et al (US Patent No. 6,264,788 B1) teach a plasma reactor including RF power sources 151 and 141 coupled to a common electrode 21, and being separated from each other via a capacitor 100 and low pas filter 144 (Fig. 6);

Tamura et al (US Patent No. 5,906,684) teach a plasma reactor including a variable DC power source 13 and an RF power source 12 coupled to a substrate holder 47 (Fig. 10);

Kaji et al (US Patent No. 5,290,993) teach a reactor including a bias power supply unit having a an RF 16 and a DC 18 power source (Fig. 1); and

Roderick et al (US Patent No. 6,074,488) teach a plasma reactor including an AC/DC unit coupled to a substrate support.

Suzuki (US Patent No. 5,777,438), Shao et al (US Patent No. 5,654,043), Ise et al (US Patent No. 6,218,196 B1), Fujiwara et al (US Patent No. 5,435,886), Wendt et al (US Patent No. 6,201,208 B1) and kubota et al (JP 11-224796 A) teach ***a pulsed bias voltage source coupled to a substrate support***.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Parviz Hassanzadeh whose telephone number is (703)308-2050. The examiner can normally be reached on Tuesday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory Mills can be reached on (703)308-1633. The fax phone numbers for the

organization where this application or proceeding is assigned are (703)872-9310 for regular communications and (703)872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0661.

P. Hassanzadeh

Parviz Hassanzadeh
Primary Examiner
Art Unit 1763

September 12, 2003